3D TSV Markets:
Applications, Issues, and Alternatives

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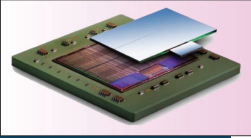

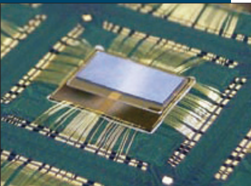

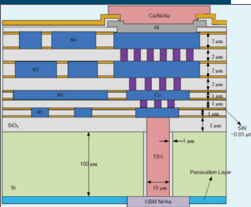

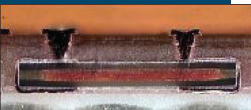

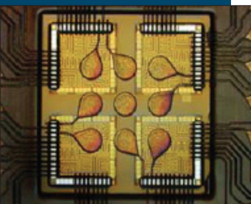

There are many approaches to 3D packages, including stacked die, stacked packages, package-on-package (PoP), and chip-on-chip (CoC). While these packaging methods provide many benefits, the adoption of 3D through silicon via (TSV) technology will enable the production of 3D ICs.

While the drivers for 3D ICs remain constant, the time line for its adoption keeps shifting out into the future. Several technical challenges and infrastructure issues such as business logistics are delaying the full commercialization of TSV technology for 3D ICs. Companies plan to continue the use of today's 3D packages with evolutionary improvements and adopt a 2.5D or interposer solution until challenges can be met.

This study provides a forecast for number of wafers and units by application with a timeline for adoption. Alternatives to 3D ICs, including the use of interposers with TSVs and continued use of PoP and stacked die with wire bond and flip chip are described. Impediments to the adoption of the technology are presented and progress in resolving issues is discussed. Full text analysis provides critical details of challenges and alternatives. The report is 122 pages with full references. A complimentary set of 78 PowerPoints accompanies the report.

Executive Summary

1 Introduction
- 1.1 Today's 3D Packages
- 1.2 Limits to Scaling
- 1.3 Drivers for 3D ICs
- 1.4 Issues for 3D ICs
- 1.5 A New Version of Multichip Module
- 1.6 Alternatives and Timing

2 Issues for 3D TSV
- 2.1 Design and EDA Tools
  - 2.1.1 EDA Tools
  - 2.1.2 Low-power Designs
  - 2.1.3 Standards Activities
  - 2.1.4 Future Needs
- 2.2 New Developments in Via Fabrication
- 2.3 Micro Bumping
- 2.4 Temporary Bond/Debond in Wafer Thinning
  - 2.4.1 Bond/Debond Equipment
    EVG, SUSS, TEL, TOK, 3M
  - 2.4.2 Materials for Wafer Bond/Debond
    Brewer Science, Dow Electronic Materials, Dow Corning, HD Microsystems, JSR, Shin-Etsu, TMAT, TOK, 3M
- 2.5 Thinning Alternatives for 3D TSV Wafers
- 2.6 Wafer Singulation
- 2.7 Flip Chip Bonding and Equipment
  Amicra Microtechnologies, ASM Pacific, Athlete FA, BESI/Datacon, FineTech, Infotech Automation, MicroAssembly Technologies, Newport MRSI, Palomar Technologies, Panasonic FA, SEC, SET, Shibaura Mechatronics, Shibuya Kogyo, Shinkawa, TDK, Toray Engineering, Tresky
- 2.8 Thermal
  - 2.8.1 3D TSVs and Heat Dissipation
  - 2.8.2 Potential Cooling Solutions
    - 2.8.2.1 Materials, Vias, and Bumps
    - 2.8.2.2 Micro-Channel Cooling
  - 2.8.3 Industry Needs
- 2.9 Test
- 2.10 Reliability
  - 2.10.1 High Performance Systems
  - 2.10.2 Mobile Products
  - 2.10.3 TSV Structures
  - 2.10.4 Reliability Data on 2.5D Structures
- 2.11 Supplier Logistics and Infrastructure

3 Alternatives to 3D TSV
- 3.1 Package-on-Package (PoP)

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3D TSV Markets:
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3.1.1 Embedded-Die PoP
ASE, AT&S, DNP, FlipChip International/Fujikura, Fujitsu, J-Devices, NANIUM, Shinko Electric, STATS ChipPAC
3.1.2 PoP Extensions
3.2 WB, FC, and Other Stacked Die Methods
Rambus, Vertical Circuits, Invensas, 3D Plus
3.3 Chip-on-Chip
Fujitsu Microelectronics, Renesas Electronics, Sony
3.4 Interposers
IBM, Xilinx, Fujitsu Microelectronics, Altera, Cisco
3.5 2.5D Interposer Suppliers
ASE, ALLVIA, DNP, IBM, IMT, IPDiA, Silex Microsystems, SPIL, STATS ChipPAC, TSMC, Tezzaron, UMC
3.6 Silicon Interposer R&D Activities
3.7 Glass Interposer R&D Activities

4 Markets and Adoption Timeframe
4.1 3D TSV by Application
4.1.1 Memory
4.1.1.1 Wide I/O Memory
4.1.1.2 DRAM Stacks with TSV
Micron, Nanya Technology, Samsung, SKHynix, Tezzaron
4.1.1.3 Flash
Toshiba, Samsung
4.1.2 GPU/CPU
4.1.3 Other Devices with 3D TSVs
4.1.4 3D Market Forecast
4.1.5 2.5D Market by Application
ASICs, FPGAs, GPUs/CPUs, Tablets, Analog Devices
4.1.6 Market Projection for 2.5D
4.1.7 Conclusions

Partial List of Figures and Tables

- 3D TSV penetration of PoP market.
- Cu pillar micro bump with SnAg cap.
- Wafer thinning and handling process.
- Thermo-slide process.
- ZoneBOND® process.
- Zero Newton® process flow equipment.
- Low-Temperature Cu-Cu Direct Bonding.
- Modular Cooling Chip Insert
- ASE's a-EASI™ substrate.
- Embedded B2it™ PoP.
- Cross-section and photograph of ChipletT™.
- Fujitsu's Embedded Die and WLP PoP
- WFOP™ structure.
- Thinner MCeP for PoP applications.
- Double-sided eWLB-PoP.
- Bond Via Array™ PoP.
- SMAFTI with TSV-stacked memory.
- Sony's CoC for the PS Vita.
- Xilinx FPGA with silicon interposer.
- Cisco's 3D SiP with TSV.
- Tezzaron silicon interposer.
- Wide I/O package configurations.
- 3D TSV Market Projections
- 2.5D Interposer Market Projections
- Commercial EDA Tools
- Micro Bump Pitch Trends
- Bond/Debond Equipment
- Materials for Bond/Debond of TSV Wafers
- Comparison of Wafer Dicing Methods
- High Precision Bonders
- Probe Card Examples
- MCM, 2.5D, and 3D TSV Comparison
- Comparison of Alternatives to 3D TSV
- Companies Offering Embedded-Die PoP
- Die Stack Examples
- Silicon Interposer Suppliers
- Fine Feature Build-up Substrate Suppliers
- 3D TSV Applications: Drivers, Status, and Barriers

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