Cost Models for Packaging

Quickly see the cost impact of design decisions

WIRE BOND

WHAT'S THE COST IMPACT OF:

Cu vs. Au wire?
Changing substrate structure—2L? 4L? Laser drilling?
Designing a smaller package?

FLIP CHIP

WHAT'S THE COST IMPACT OF:

Using a smaller package with a more complicated structure?
Including discrete devices in the package?
Using a larger die?

WLP

WHAT'S THE COST IMPACT OF:

Fan-in versus fan-out?
Embedded die?
Additional RDL layers?

SUPPLIER SPECIFICS

An optional enhancement is to create a model calibrated to your particular technology or to a specific supplier (internal or external). Ask us for more details.

We have models for wire bond, flip chip, and WLP applications. Many detailed parameters are available for editing, but only a few inputs are required to run the analysis. For parameters you choose not to edit yourself, complex SavanSys algorithms automatically assign default values based on your other entries and extensive, up-to-date industry knowledge.

Use the model to:

- Define characteristics of the assembly site, fabrication site, and design.
- Compare against your previous results to easily understand how your cost changes.
- View the detailed costs—including labor, material, capital, tooling, and yield impacts—of every step.

Sample parameter list:

Design
Package size
I/O count
Die size and cost
Stacked die?
Wire options
Wafer bumping method
Design rules
Material
Core thickness
BGA pitch
Wire count
Microvia count
Capacitor details
PTH count
Heat spreader or stiffener
Mold compound
Surface finish
Process

Assembly Factory
Labor rate
Lot size
Annual volume
Wafer probe yield
Factory utilization
Cost of gold
Strip size
Overhead rate

Substrate Factory
Labor rate
Lot size
Factory utilization
Panel size
Overhead rate

The models are the result of a joint project between TechSearch International, Inc., the leading market research firm in semiconductor packaging and assembly trends, and SavanSys Solutions LLC, the leader in electronic manufacturing cost modeling.

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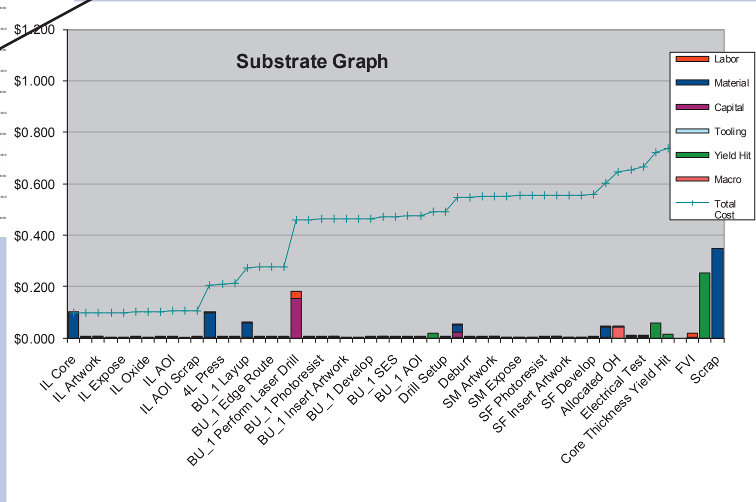
Assembly Parameters	Input	Value Used	Comments
Assembly Location	Taiwan	Taiwan	
Fabrication Parameters			
Fabrication Location	Taiwan	Taiwan	
Known substrate cost	Default		
Factory utilization	Default	85.00%	
Panel Length (in)	Default	16.00	
Panel Width (in)	Default	18.00	
Lot Size	Default	20	
Substrate Cu Pillars	Default	None	
Design Parameters			
Package Size	29x29	29x29	
Package I/O Count	900	900	
Substrate Structure	1-4-1	1-4-1	
Die Options			
Die Length (mm)		14.500	
Die Width (mm)		14.500	
Die Thickness (mm)		1.200	
Die Cost		$0.000	
Die Pad Pitch (um)		200	
Package Options			
Line and Via Design Rule	Default	Mainstream	
Stacked Vias	Default	No	
Surface Finish	Default	ENIG	
Material (Factor)	Default	1	

6-2-6
0-4-0
1-4-1
2-4-2
3-4-3
4-4-4
5-4-5
6-4-6

Customize parameters across assembly, fabrication, and design.

Select/Input values yourself
OR
Let SavanSys provide appropriate



Graph displays detailed cost for every process step, including: Labor, Material, Tooling, Yield loss, and more.

Fax to 512-372-8889 or email to tsi@techsearchinc.com

Name: ______________________ Email: ______________________

Position: ______________________ Telephone: ______________________

Company: ______________________ Fax: ______________________

Ship to Address: ______________________ Bill to Address: ______________________

Price per model for a single-user license (annual): $3,750.00

Price per model for a corporate license (annual): $12,500.00

Check the model(s):
you want to purchase

Single-user license	Flip Chip ☐	Wire Bond ☐	WLP ☐
Corporate license	Flip Chip ☐	Wire Bond ☐	WLP ☐

Purchase order number: ______________________

AMEX, VISA, MC, JCB: ______________________ Exp: __________

Total amount: ______________________