# 2.5D & 3D Packaging Cost Model

## Which applications are right for this technology?

This is the first cost model to cover the total cost and yield from fabrication of the wafer to complete assembly, for both 2.5D and 3D applications. Many detailed parameters are available for editing, but only a few inputs are required to run the analysis. For parameters you choose not to edit yourself, complex SavanSys algorithms automatically assign default values based on your other entries and extensive, up-to-date industry knowledge.

Use the model to:

- Compare the cost of 2.5D and 3D packaging to see what makes sense for your product.
- Include supplier specific details and incoming die preparation in your analysis.
- View the detailed costs—including labor, material, capital, tooling, and yield impacts—for every step.

### Sample parameter list:

**Design**
2.5D process flow (chip-on-chip/wafer/substrate)
Number of Die
Interposer size
Number of RDL
TSV Aspect Ratio
Number of TSV per Die

**Preparation of Die**
Incoming Wafer Cost
Location/Labor Rate
Die Size

**Supplier Settings**
Labor rate
Lot size
Overhead rate
Margin/Risk factor
Factory utilization

**Advanced**
TSV formation process type
TSV formation yield
RDL creation process type
Underfill process
….and more

*TECHNOLOGY TRADE-OFFS*
**WHAT'S THE COST IMPACT OF:**
- Additional RDL layers?
- Higher costs, better yield?
- Increasing TSV Count?
- Interposer versus true 3D?

*COST BREAKDOWN*
**SUMMARIZE TOTAL COST**
- Results are broken down into FEOL, BEOL, TSV creation and assembly.
- Wafer cost and unit cost are presented separately.
- Risk and yield are included in the total cost.

*PROCESS DETAILS*
**COMPLETELY CUSTOMIZABLE**
- Disable specific process steps.
- Account for test activities.
- Customize process steps with known data (equipment cost, throughput, material, and more).

**SUPPLIER SPECIFICS**
An optional enhancement is to create a model calibrated to your particular technology or to a specific supplier (internal or external). Ask us for more details.

This model is the result of a joint project between TechSearch International, Inc., the leading market research firm in semiconductor packaging and assembly trends, and SavanSys Solutions LLC, the leader in electronic manufacturing cost modeling.


the SavanSys solution

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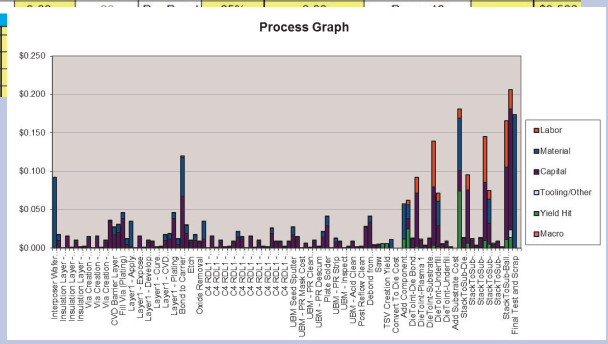
| Design Options | | |
|---|---|---|
| Configuration | Interposer | Interposer |
| Integration | Chip-on-Chip | Chip-on-Chip |
| # of Die | 2 | 2 |
| Package Size | 27x27 | 27 x 27 |
| ***Interposer*** | | |
| Interposer Size | 12x12 | 12 x 12 |
| # Interposer to Die RDL | 1 | 1 |
| # Interposer to Substrate RDL | 1 | 1 |
| ***TSV*** | | |
| # TSV Per Die | 100 | 100 |
| TSV Diameter (um) | 10.00 | 10.00 |
| TSV Depth (um) | 90.00 | 90.00 |
| TSV Aspect Ratio (calcula | 9.00 | |

| Results | Current | Previous Run |
|---|---|---|
| Total Package Cost | **$0.000** | *$0.000* |
| Die To Interposer Ass | $0.000 | *$0.000* |
| Interposer to Substrat | $0.000 | *$0.000* |
| Integration Costs | $0.000 | *$0.000* |
| etc… | $0.000 | *$0.000* |
| Interposer Yield | 0.00% | *0.00%* |
| Package Yield | 0.00% | *0.00%* |

| Supplier Settings | Fab 1 |
|---|---|
| Labor Rate | Taiwan |
| Factory Utilization | 85% |
| Lot Size / Batch Size (# Wafe | 12.00 |
| Overhead/Indirect % | 110.00% |
| Margin/Risk Factor % | 40.00% |

| Step Name | Enabled? | Time (min) | Through put (UPH) | Time Units | Operator Utilizatio n | Defect Density or PPM | Defect Density Units | Step Yield | Equipm Cos |
|---|---|---|---|---|---|---|---|---|---|
| [01] Interposer Wafer Cost | YES | 0.00 | | Per Panel | 25% | 0.00 | Per cm^2 | | $0 |
| [11] Insulation Layer - CVD | YES | 2.00 | 30 | Per Panel | 25% | 0.00 | Per cm^2 | | $2,500 |
| [11] Insulation Layer - Mask Cost | YES | 0.00 | | Per Lot | 25% | 0.00 | Per cm^2 | | $0 |
| [11] Insulation Layer - Expose | YES | 2.00 | 30 | Per Panel | 25% | 0.00 | Per cm^2 | | $4,000 |
| [11] Insulation Layer - Clean Mask | YES | 5.00 | 12 | Per Lot | 100% | 0.00 | Per cm^2 | | $1,000 |
| [11] Insulation Layer - Etch | YES | 20.00 | 3 | Per Lot | 25% | 0.00 | Per cm^2 | | $2,500 |
| [11] Insulation Layer - Cure | YES | 90.00 | 1 | Per Lot | 25% | 0.00 | Per cm^2 | | $100,0 |
| [11] Insulation Layer - Descum | YES | 1.00 | 60 | Per Panel | 25% | 0.00 | Per cm^2 | | $750,0 |
| [11] Via Creation - Photoresist | YES | 2.50 | 24 | Per Panel | 25% | 0.00 | Per cm^2 | | $2,500 |
| [11] Via Creation - Mask Cost | YES | 0.00 | | Per Lot | 25% | 0.00 | Per cm^2 | | $0 |
| [11] Via Creation - Expose | YES | 2.00 | 30 | Per Panel | 25% | 0.00 | Per cm^2 | | $4,000 |
| [11] Via Creation - Clean Mask | YES | 5.00 | 12 | Per Lot | 100% | 0.00 | Per cm^2 | | $1,000 |
| [11] Via Creation - Develop | YES | 20.00 | 3 | Per Lot | 25% | 0.00 | Per cm^2 | | $2,500 |
| [11] Deep Reactive Ion Etch | YES | 5.00 | 12 | Per Panel | 50% | 0.00 | Per cm^2 | | $3,500 |
| [11] CVD Barrier Layer | YES | 2.50 | 24 | Per Panel | 25% | 0.00 | Per cm^2 | | $3,500 |
| [11] PVD Cu Seed Layer | YES | | | | | | | | |
| [11] Fill Via (Plating) | YES | | | | | | | | |
| [11] CMP | YES | | | | | | | | |
| [12] Layer1 - Apply Dielectric | YES | | | | | | | | |
| [12] Layer1 - Mask Cost (Trench) | YES | | | | | | | | |
| [12] Layer1 - Expose (Trench) | YES | | | | | | | | |




Enter values (or let SavanSys select default values) on the main page to construct the initial process.

After constructing and running the process based on your initial inputs, view/edit the details of every processing step.

Results are presented as a summary on one page, and also as a detailed graph (shown here).

Fax to 512-372-8889 or email to tsi@techsearchinc.com

Name: _____ Email: _____

Position: _____ Telephone: _____

Company: _____ Fax: _____

Ship to Address: _____

_____

_____

Bill to Address: _____

_____

_____

Price per model (annual corporate license): $12,500.00

☐ I want to purchase the 2.5D & 3D Packaging Cost Model

Purchase order number: _____

AMEX, VISA, MC, JCB: _____ Exp: _____

Total amount: _____