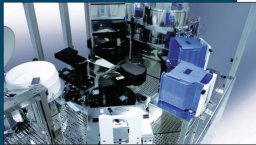
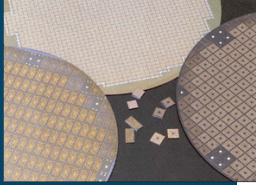


# WLP Trade Off Cost Model



The Wafer Level Packaging Trade Off Cost Model allows users to easily analyze the cost and yield results of the following three WLP technologies.

- Fan-in WLP - Package size is the same as the die size
- Fan-out WLP - Larger package fabricated around the die using semiconductor processing technology
- Embedded die - Larger package fabricated around the die using PCB technology

By limiting the number of required inputs while maximizing the number of optional parameters, customers can examine WLP options to determine cost impacts of each. The model is the result of a joint project between TechSearch International, Inc., the leading market research firm in semiconductor packaging and assembly trends, and SavanSys Solutions LLC, the leader in electronic manufacturing cost modeling. The model is a comprehensive activity based model and its accuracy has been validated using dozens of industry data points.

Use the estimator to optimize your technology selection:

- Compare packaging cost, die cost, and yield for packages fabricated using three WLP technologies—Fan-in WLP, Fan-out WLP, and Embedded die
- Accurately quantify the cost of technology choices—fan in or fan out, package size, UBM choice, ball diameter and pitch, number of redistribution layers, etc.
- Understand and manage your detailed costs—labor, material, capital, tooling, and yield impacts—for every step in the wafer level packaging process

Optimize your cost by selecting the right supplier:

- Trade off manufacturing locations
- Obtain the “should cost” value for your package

An optional enhancement is the creation of a model calibrated to a specific supplier (internal or external). Our team of professionals can work with you to calibrate the model, or work directly with the supplier to create a supplier certified model.

The list of model parameters is as follows:

<b>Manufacturing location</b>	<b>Die pad pitch</b>
<b>Factory utilization</b>	<b>BGA pitch</b>
<b>Semiconductor defect density</b>	<b>Solder ball diameter</b>
<b>Semiconductor wafer cost</b>	<b>Ball attach method</b>
<b>Wafer diameter</b>	<b>Number of redistribution layers</b>
<b>Package size</b>	<b>Dielectric processing defect density</b>
<b>Package I/O count</b>	<b>Metal processing defect density</b>
<b>Die length / width</b>	<b>Die placement yield</b>
	<b>Allocated overhead/profit</b>

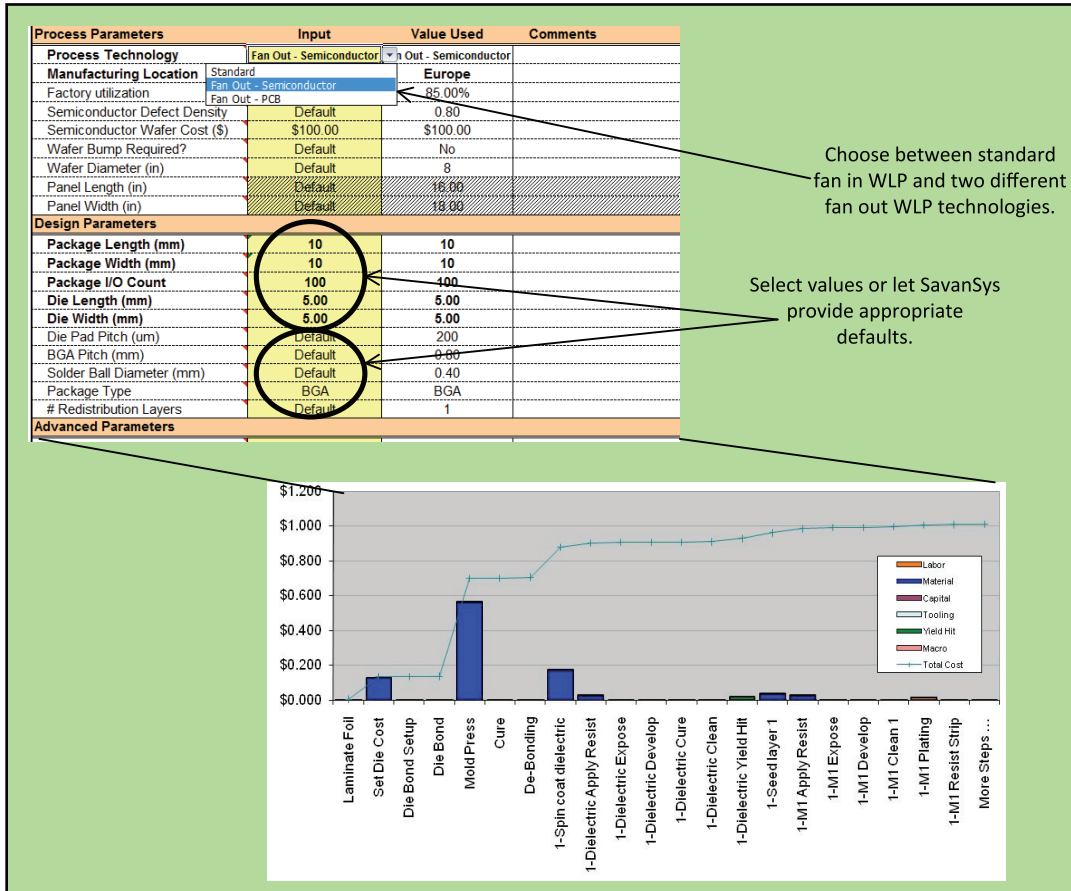
the **SavanSys**  
solution

SavanSys Solutions LLC  
10409 Peonia Ct.  
Austin, TX 78733  
512-402-9943  
info@savansys.com  
www.savansys.com

**TechSearch**  
INTERNATIONAL

4801 Spicewood Springs Road • Suite 150  
Austin, Texas 78759  
Tel: 512-372-8887 • Fax: 512-372-8889  
tsi@techsearchinc.com • www.techsearchinc.com

# WLP Trade Off Cost Model



Fax to 512-372-8889 or Email to [tsi@techsearchinc.com](mailto:tsi@techsearchinc.com)

Name: \_\_\_\_\_

Position: \_\_\_\_\_

Company: \_\_\_\_\_

Ship to Address: \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

Email: \_\_\_\_\_

Telephone: \_\_\_\_\_

Fax: \_\_\_\_\_

Bill to Address: \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

Purchase Order Number: \_\_\_\_\_

AMEX, Visa, MC, JCB: \_\_\_\_\_

Annual Model Price: \$ 2,500.00

Total Amount: \$ \_\_\_\_\_

Exp. Date: \_\_\_\_\_