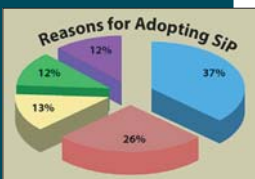
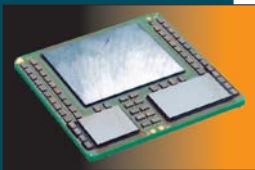
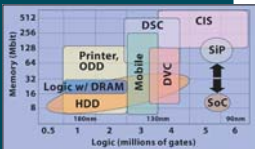


# System-in-Package: The New Wave in 3D Packaging



Technology advances and market drivers have produced a renaissance in multichip packaging solutions. System-in-Package (SiP) solutions are increasingly found in a broad range of market segments, including consumer electronics such as digital cameras and camcorders, automotive, military/aerospace, medical, computer, and telecommunications products. Each market segment has particular needs and drivers that require a diverse set of structures and configurations. SiP examples are provided, including details on the number and type of die, package type and body size, configuration, lead count, and substrate. Drivers for the use of SiP in each application area are described, along with performance requirements and functions.

The report answers the key question of how SiPs are different from multichip packages of the past. One application—wireless products—stands out as a high-volume driver that did not exist a dozen years ago when many multichip packages were first introduced. SiPs deliver increased functionality and performance in small form factor for mobile communication, resulting in significantly greater adoption rates than any previous multichip module. A variety of SiPs are found in the RF, digital baseband, and transceiver sections of mobile phone. Emerging applications for mobile phones include mini hard disks and camera modules. Both planar and stacked configurations are in use and several companies, including Philips, STMicroelectronics, and SyChip, have introduced integrated passive substrate solutions.

A five-year industry outlook and projections by market are provided for each application. With a unit growth rate of almost 20 percent CAGR between 2004 and 2009, semiconductor designers and fabs, along with substrate providers, assembly houses, circuit board manufacturers, EMS companies, and systems houses are experiencing the benefits of SiP and the changes brought about by its use. Each facet of the SiP supply chain, including design, procurement, manufacturing, assembly, and test, is analyzed. New concerns, including logistical and engineering issues, wafer thinning, and assembly, are addressed. The report explains how the issue of KGD has driven the development of new package configurations such as package-on-package and package-in-package. An insight into the relationship between SiP and system-on-chip (SoC) as both competing and complementary solutions is also included.

## Executive Summary

- SiP Emerges
- SiP Applications
- Key Issues for SiP

## 1 Introduction

- 1.1 History of Multichip Packaging
  - The First Wave - MCMs
    - A Definition for MCM
  - The Second Wave - MCPs
    - A Definition for MCP
  - Benefits of Multiple Chip Packaging
  - IC Integration - The SoC Movement
  - The New Wave - SiPs
    - Single Chip Packaging
    - Stacked Die Package
    - SiP Definition
    - SiP Packaging Alternatives
    - SoC versus SiP

## 2 Markets and Applications

- 2.1 Mobile Phones and Wireless Products
  - Stacked Die Packages
  - Global Positioning Systems
  - Camera Modules
  - Mini Hard Disk
  - Future Packages
  - Wireless SiP Market Projections
- 2.2 Consumer Products



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## 2.3 MP3 and DVD Players

## 2.4 Home Appliances

- Consumer Product SiP Market Projections

## 2.5 Medical Electronics

- Ultrasonic Diagnostic System
- Capsule Endoscopy
- Hearing Aids
- Implantable Products
- Future Applications
- Medical SiP Market Projections

## 2.6 Computing Hardware

- Personal Computing
- Supercomputers/Mainframes/Servers
- FPGA Modules
- Graphics Modules

## 2.7 High Performance Networking Hardware

- Computer / Communication SiP Market Projections

## 2.8 Automotive Electronics

- Automotive SiP Market Projections

## 2.9 Defense and Aerospace Electronics

- Military/Aerospace SiP Market

## 3 Design

### 3.1 Issues and Challenges in Design

- 2D versus 3D Layout
- Modeling and Simulation
- Cost Modeling

### 3.2 State of the Industry

- Design Strategies
- The Gap in Design, Modeling, and Simulation Tools

## 4 Interconnect and Assembly

### 4.1 Assembly Issues and Trends

- Die Thinning
- Die Attach
- Interconnect Methods

- Substrates

## 4.2 Thermal Issues

## 4.3 Future Requirements

## 4.4 Impact of Environmental Requirements

## 5 Test

### 5.1 Single-Chip Module Process

### 5.2 Packaging of Multiple Devices

- Known Good Die
  - Die Level KGD Technology
  - Wafer Level KGD
  - Statistical Test Methods and Reliability Screens
  - BIST
  - Issues with KGD
  - KGD Strategies for SiP
- Substrate Test
- Module Test
- Design for Test and Test Strategies

### 5.3 Warranty

## 6 Contract Manufacturing

### 6.1 Unique Challenges of SiP Production

- Component Traceability
- Rework

### 6.2 Strengths of SATS and EMS Providers

## 7 Future Technology

### 7.1 Industry Roadmap for SiP

### 7.2 3D Integration Wafer-to-Wafer Bonding

- Through-hole Vias
- Wafer-to-Wafer Bonding

### 7.3 System-on-Package

### 7.4 Ambient Intelligence

## Appendix A: Assembly and Test

## Appendix B: Substrates

### System-in-Package: The New Wave in 3D Packaging

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