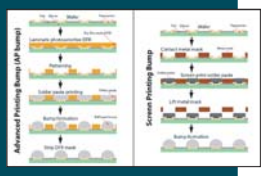
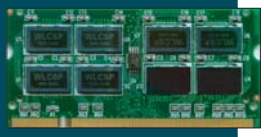
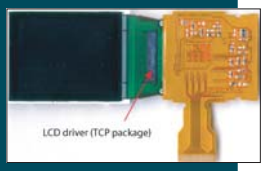
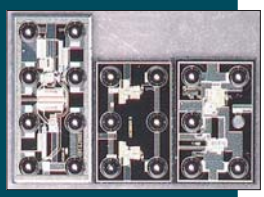
Flip Chip and Wafer Level Packaging Trends and Market Forecasts









Demand for flip chip bumping and wafer level packaging is growing rapidly. Increasing shipments of processors, ASICs, field programmable gate arrays (FPGAs), chip sets, graphics devices, and high-end DSPs are driven by the need for improved performance. Form factor needs are driving greater adoption of flip chip in CSPs. Trends include the use of flip chip for silicon with low-k dielectrics, 300mm wafer bumping, adoption of lead-free bumping, and new underfill materials and methods. New applications are described. This analysis provides an updated forecast of the flip chip wafer bumping market by product application, device type, bump type, die size, number of wafers, and number of die. Included are projections for capacity (merchant and captive) and demand. Capacity is projected by number of wafers and bump type. WLPs are also growing in volume with shipments of integrated passives, power amplifiers, battery management devices, controllers, image sensors, diodes, filters, memory (DRAM, flash, SRAM), and power MOSFETS. Projections for wafer level packages (WLPs) are provided in both units and number of wafers. New applications are discussed.

TechSearch INTERNATIONAL

4801 Spicewood Springs Road • Suite 150
Austin, Texas 78759
Tel: 512-372-8887 • Fax: 512-372-8889
tsi@techsearchinc.com • www.techsearchinc.com

Flip Chip and Wafer Level Packaging Trends and Market Forecasts

List of Figures

List of Tables

To order your copy now, you can download an order form at http://www.techsearchinc.com/pdfs/orderformGeneric.pdf or contact Becky Travelstead at 512-372-8887.