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Trends in Advanced Packaging

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Advanced Packaging Market: Remains Positive

- Advanced Packaging includes BGAs, CSPs, flip chip, and wafer level packages (WLPs)
- Still shows growth, despite the global recession
- Accounted for 30% of the 162 billion integrated circuits shipped in 2008
- Projected to account for 44% of the 205 billion IC market projected by IC Insights in 2012
- Despite cuts in CAPEX, some investment in Advanced Packaging will continue
  - Capacity for 300mm bumping and wafer level packaging is tight (regional shortage)
  - Fanout WLP experiencing growing demand
  - 3D die stacking with through silicon via (TSV) moving from R&D to prototypes

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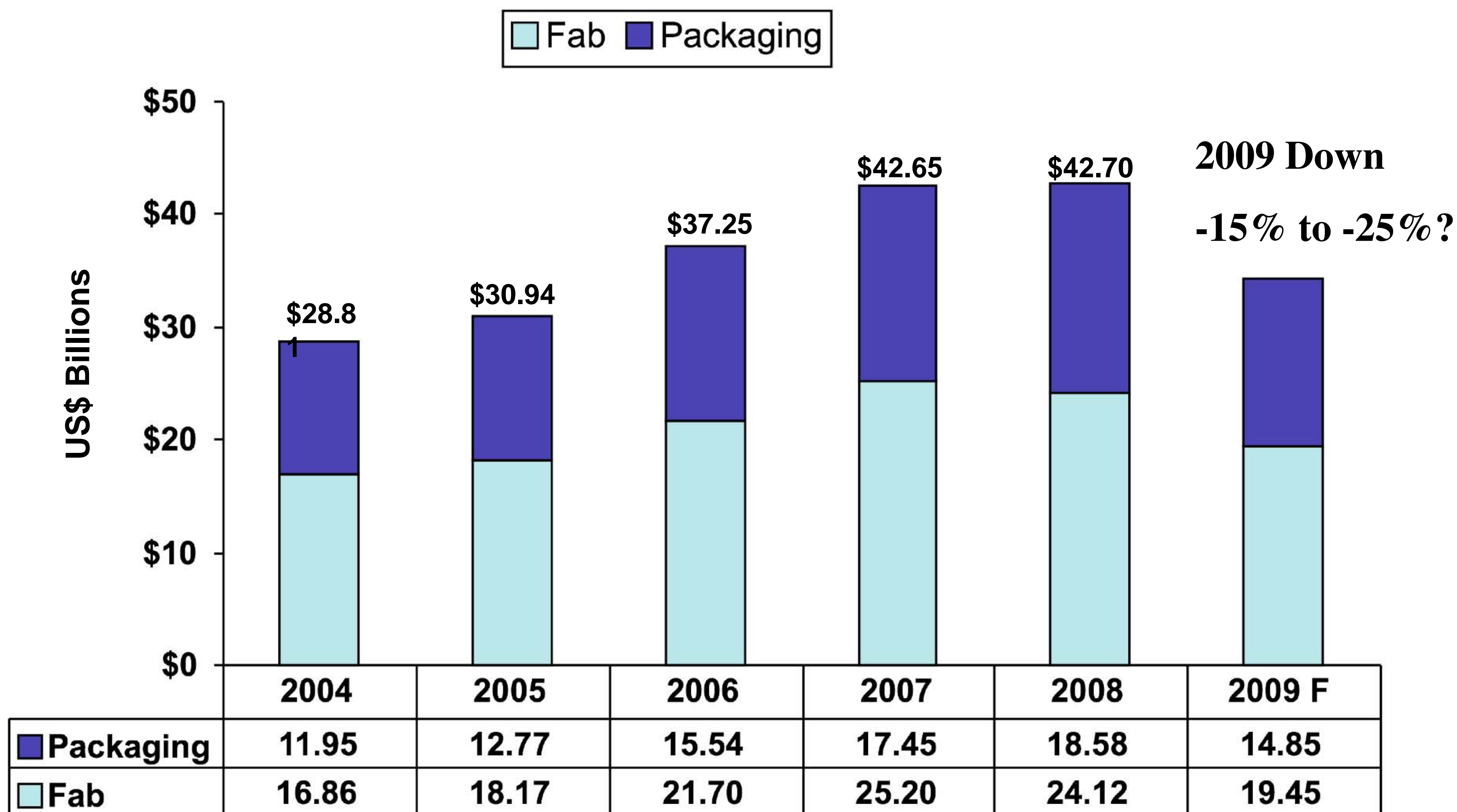
Materials Market Forecast By Segment



	2004	2005	2006	2007	2008	2009 F
Packaging	11.95	12.77	15.54	17.45	18.58	14.85
Fab	16.86	18.17	21.70	25.20	24.12	19.45

Totals may not add due to rounding.

Source: SEMI February 2009

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Growing Importance of Laminate Substrates

- The SEMI/TechSearch International Global Semiconductor Packaging Material Outlook shows laminate substrates key part of the total market
  - Laminate IC packages expected to account for 38% of the total semiconductor packaging material market for 2009
  - Includes flip chip substrates, wire bond substrates, and CSP substrates
  - Flip chip substrate prices drive the higher dollar value
- Laminate substrates account for an increasing number of IC packages
  - Microprocessors for personal computers etc.
  - Chipsets, ASICs, graphics, and many high performance devices
  - DRAM shift leadframe packages (TSOPs) to laminate CSPs (FBGA is reference package for DDR3)
- Market continues to grow for laminate substrates

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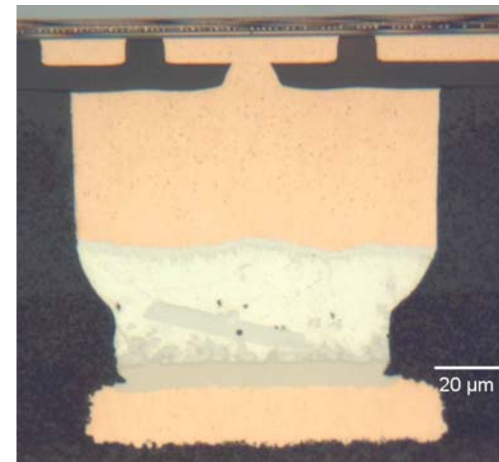
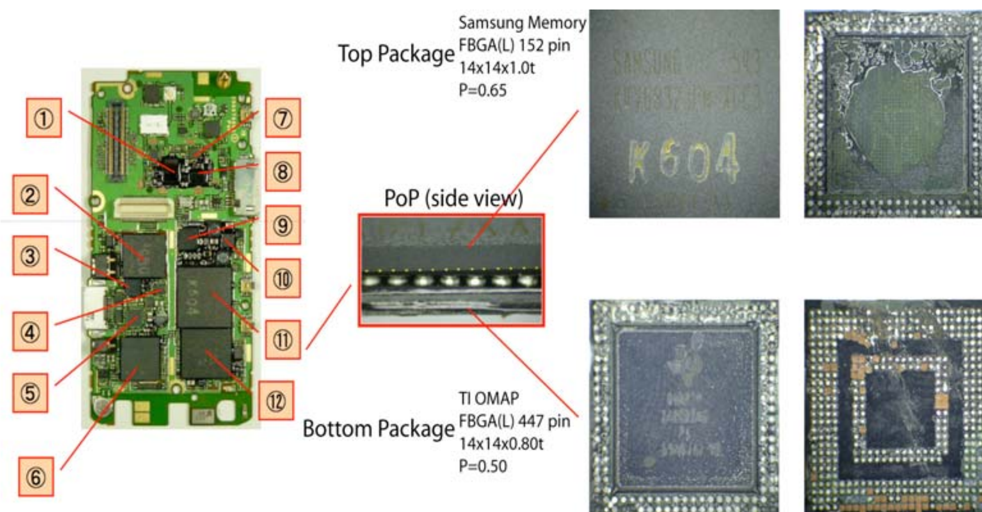
Flip Chip Growth Drivers

- Flip chip growth for high performance devices
  - Microprocessors
  - ASICs, FPGAs, and DSPs
  - Chipsets and Graphics
- Future flip chip growth in wireless products
  - Driven by form factor and performance
  - Baseband processors moving to flip chip
  - Bottom package in PoP



Source: Chipworks



Source: TPSS.

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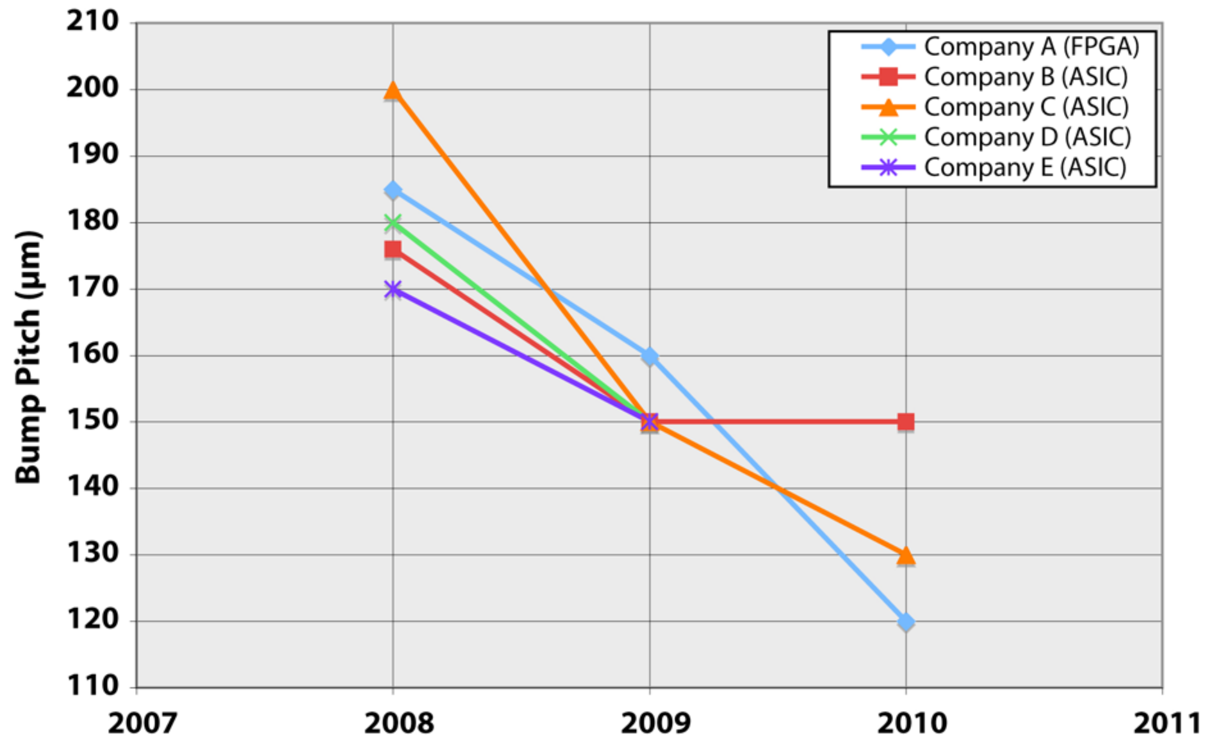
Solder Bump Pitch Trends



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Trends Impacting Laminate Substrates

- Flip chip IC bump pitch
  - 170-200µm today moving to 150-160µm in next generation
  - Cu pillar moving to as fine as 130-150µm in 2009-2010
- Shift to Pb-free bumps
  - Finer pitch bumps
  - Higher reflow temperatures
- Introduction of lower-k dielectrics and Pb-free will be challenging
- Substrate developments
  - Higher density, thin core substrates
  - Not much change for design rules this year
- Substrate finishes
  - Moving away from Electroless Nickel Gold (ENIG)
  - Adoption of Electroless Nickel, Electroless Palladium Gold (ENEPG)
  - Copper finish, OSP, immersion Sn, or SOP options

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Other Substrate Types

- Ceramic
  - High-performance MCMs for mainframes and servers
  - Telecommunications switching
  - Network computing
  - Military and aerospace
- Thin Film on Silicon or Glass
  - Introduced for MCMs many years ago
  - Today's volume production includes integrated passives for wireless applications
  - IBM's recent introduction
  - Many research programs looking at silicon substrates

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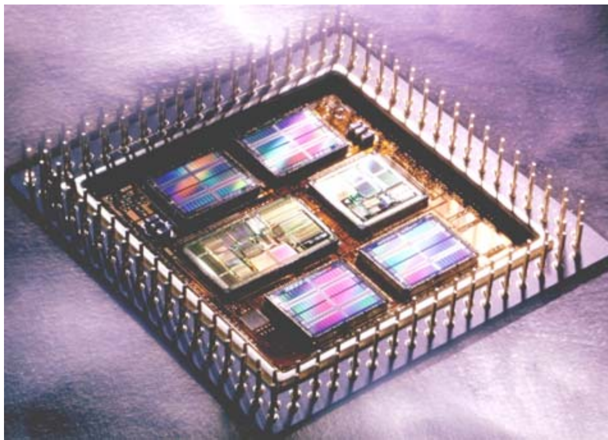
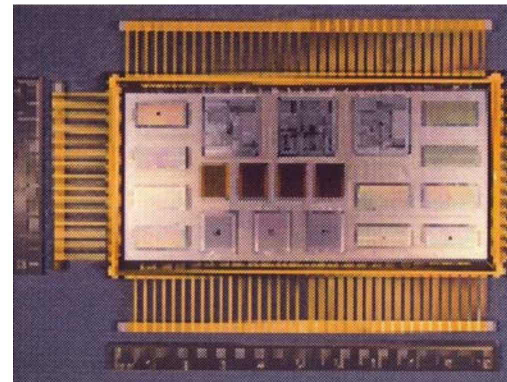
History of Silicon Substrates

- **Early developments from AT&T Bell Labs, IBM, Toshiba, NEC, and others**
- **Large Panel MCM-D Consortium (Glass)**
- **Thin Film on Silicon Substrates**
  - **Intel**
  - **IBM**
  - **Micro Module Systems (MMS)**
  - **nChip**
  - **Many Japanese companies such as Toshiba and NEC**



Source: MMS



Source: nChip

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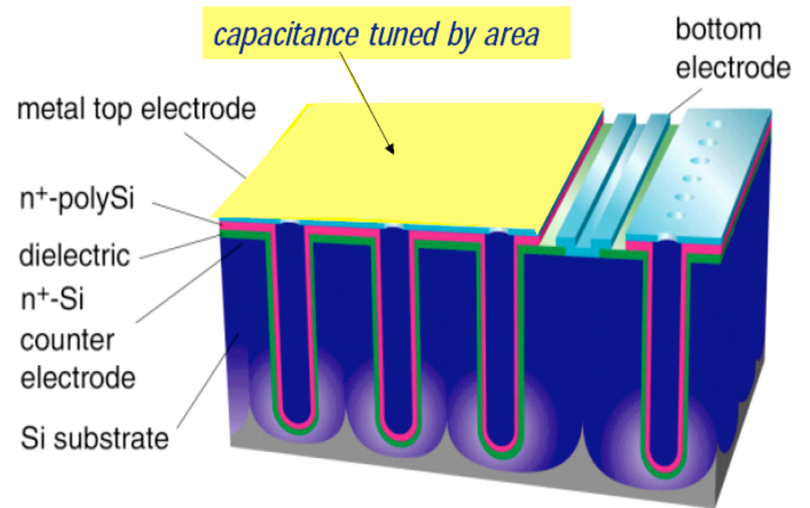
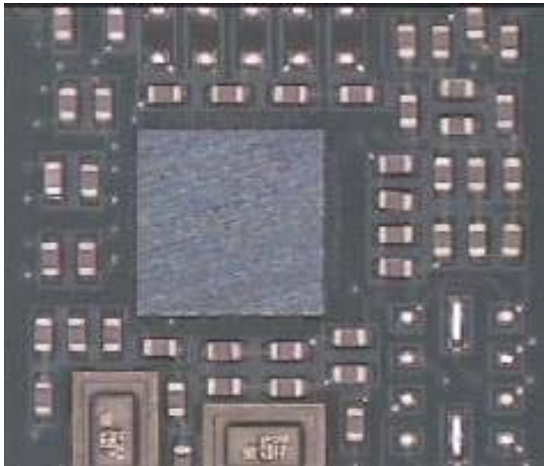
Integrated Passives in Silicon Substrates

- **Early developments from AT&T Bell Labs and Intarsia**
- **Thin film process on silicon or glass**
  - **STMicroelectronics**
  - **SyChip**
  - **IPDIA (spin out from NXP)**
- **Active devices mounted on top of substrate**
- **Discrete passive devices may also be mounted**
- **System cost savings**
- **Smaller form factor**



Source: NXP (IPDIA)



Source: STMicroelectronics

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Silicon Substrates

- Advantages
  - Fine features of less than 20µm line and space are possible
  - High density interconnect with small footprint
  - Short connections for high speed digital silicon chip
  - Excellent decoupling and grounding (close to the silicon chip)
  - Can minimize line parasitic capacitance, line length variation, and other issues associated with high-frequency designs
  - Can embedded passives
  - Can do through silicon via (TSV)
- Disadvantages
  - Cost
  - Few suppliers

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Where Are We with TSV Applications?

- TSV in high volume production for image sensors
  - Toshiba's image sensor
- More than 50 research organizations with active programs
- Drivers include severe interconnect delay for high performance devices
  - Noted in the revised ITRS roadmap
  - Serious interconnect delay for 32nm CMOS technology
  - Bottleneck for higher bandwidth microprocessor with multi-core processing
- Cost/Performance Trade-off Determines Adoption for Each Application
- Issues with TSV expansion
  - Design partition (floorplanning, routing, power/signal integrity)
  - Thermal integrity
  - Testing options (KGD, yield, test methods)

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WLP Trends

- Major application for WLP driven by mobile phones
  - Provides smaller, thinner package
  - WLPs found in almost all phones from high-end to low-end handsets
- Consumer products and other applications
  - Digital cameras and camcorders
  - Watch modules
  - Laptop computers
  - Medical
  - Automotive
- WLPs for many device types
  - WLPs for analog functions, power management, RF, wireless LAN, integrated passives, sound IC
- New WLP technologies being introduced
  - Fan-out WLPs
  - Increasing use of TSV in some applications

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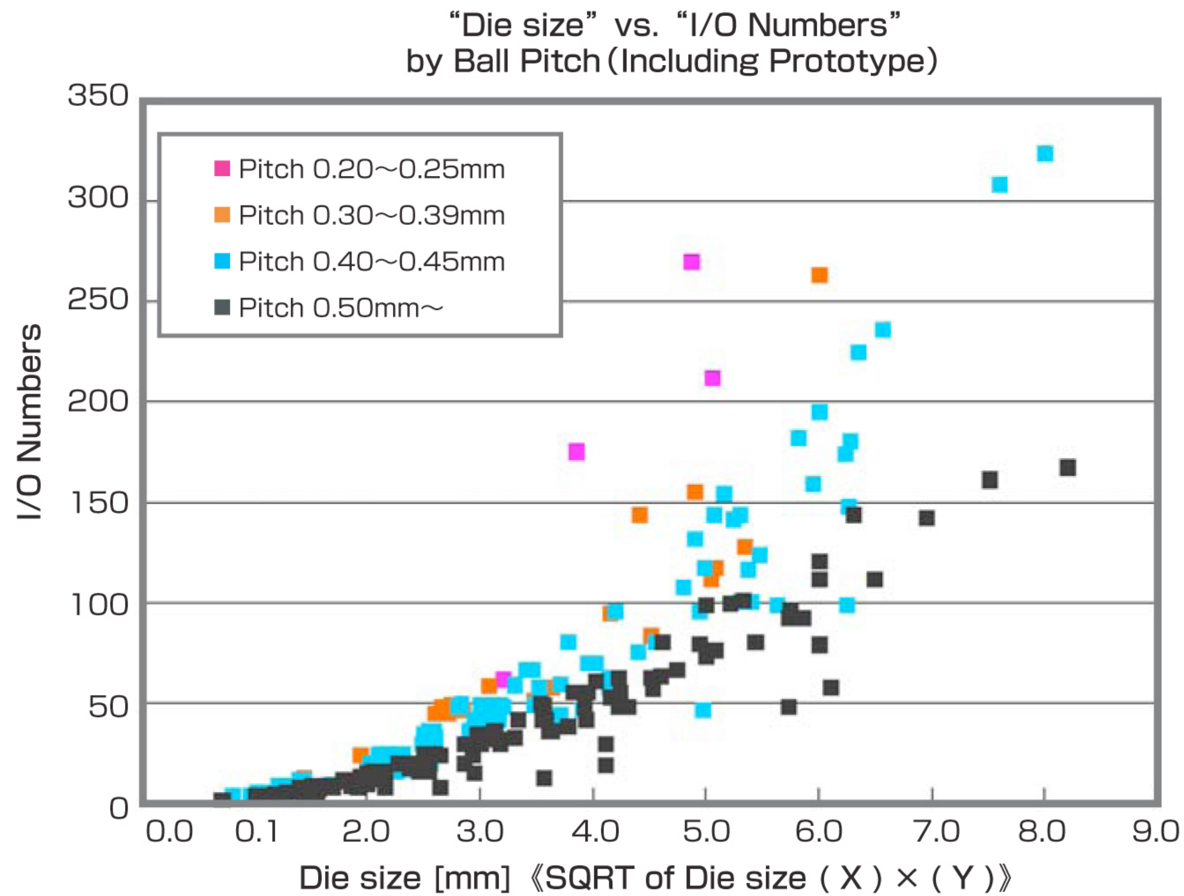
Casio's WLP Examples



Source: Casio Micronics

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Semiconductor Packaging Material Developments

- Wire bonding
  - Shift to copper wire with higher price of gold
- Underfill materials
  - Majority remains capillary flow
  - Interest in mold compound as underfill
- WLP dielectrics
  - Increased demand for WLPs
  - Higher pin counts driving adoption of Fan-out WLP with mold compounds

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Conclusions

- Advanced packaging continues to drive unit volume growth and revenue growth
- Flip Chip Growth
  - Increasing in unit volumes, FCIP highest growth rate
  - Assembly of flip chip is higher margin business for assembly and packaging industry
- Portable products increasing use of flip chip and WLP especially wireless applications
  - Many new packages are under development including fanout WLP
  - Solder bump and copper pillar growth continues
- WLP growth driven by need for thinner, smaller packages in mobile phones
  - CAPEX for new lines
  - Capacity for 300mm WLP tight in some regions
- 3D TSV is still a "hot technology"
  - Many companies moving from research to commercialization
  - Almost 50 organizations identified with 3D TSV activities
  - Cost/performance trade-offs major factor in determining timing
  - Industry working on design software and test issues

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