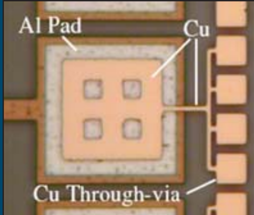
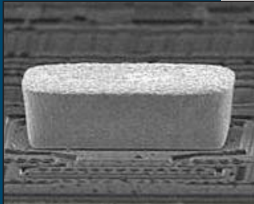
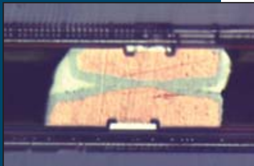
3D Integration at the Wafer Level

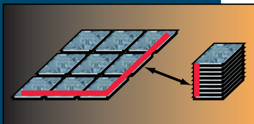


Driven by the need for improved performance, a number of companies are researching methods to use short vertical interconnections to replace the long interconnects found in 2D structures. Stacking disparate technologies to provide a structure with potential functions including logic, memory, MEMS, antennas, display, RF, analog/digital, sensors, and power storage is potentially possible with 3D heterogeneous integration, making this technology the "Holy Grail" of system integration. The new 3D options include both wafer-to-wafer stacking and chip-to-wafer stacking. This analysis highlights the drivers for the technology and the activities of companies, research organizations, and universities.



Key in the development of the technology is the use of through wafer vias, wafer thinning, and the ability to bond these new structures. Through wafer via options include deep etch capability such as the anisotropic "Bosch etch." Innovative solutions are being developed by a number of companies and include insulator formation by CVD TEOS or polymers. Conductor options include copper, tungsten, or poly silicon. Wafer thinning features lapping/grinding followed by wet etch, plasma etch, or CMP. Bonding options include silicon or metal fusion, Cu/Sn eutectic, polymer bonding, and bumping.





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3 Commercial 3D Integration Activities
IBM, Infineon, Intel, Micron, Oki Electric, Philips, Renesas, Samsung Electronics, Tezzaron Semiconductor, Toshiba, Ziptronix, ZyCube, Association of Super Advanced Electronic Technologies, Cornell, Defense Advanced Research Projects Agency, IMEC, Fraunhofer-IZM Munich, Lincoln Labs, Massachusetts Institute of Technology, Rensselaer Polytechinc Institute, Research Triangle Institute, Sandia National Labs, International SEMATECH, Tohoku University, University of Arkansas

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3D communication processor.
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