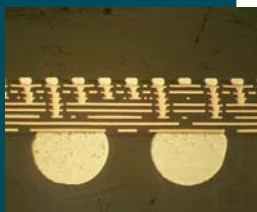
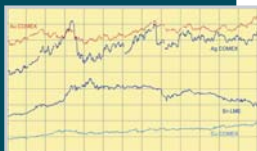


Advanced Packaging Update: Market and Technology Trends

Q2, 2005



The second quarterly Advanced Packaging Update for 2005 features a special section on IC package assembly price trends. The industry is experiencing assembly price increases of 10 to 15 percent on average for almost all packages. Assembly capacity is tight and some companies are experiencing difficulty finding suppliers willing to provide assembly services for small volumes. The section includes an analysis on the factors driving the price increases. The report also features coverage of flip chip substrate developments. Descriptions of flip chip substrates offered by companies worldwide are provided. Industry trends for laminate flip chip substrates are discussed, including body size, core thickness, via and pad diameter, minimum bump pitch supported, and substrate finish. Trends in RoHS compliance are also provided.

Table of Contents

- 1 IC Package Assembly Price Trends**
 - QFPs, Wire Bond PBGAs, Flip Chip PBGAs, Laminate CSPs, Lead Frame CSPs
- 2 Flip Chip Substrates**
 - 2.1 ASE, Inc.
 - 2.2 Compeq Technologies
 - 2.3 Daisho Denshi America, Inc.
 - 2.4 Endicott Interconnect Technologies
 - 2.5 Fujitsu Interconnect Technologies
 - 2.6 Ibiden Company, Ltd.
 - 2.7 Japan Circuits Industrial Company
 - 2.8 Kinsus Interconnect Technology Corp.
 - 2.9 Kyocera SLC Technologies
 - 2.10 Mitsui Chemicals America, Inc.
 - 2.11 NEC Toppan Circuit Solutions, Inc.
 - 2.12 Nan Ya Printed Circuit Board Corp.
 - 2.13 NTK Technologies, Inc.
 - 2.14 Phoenix Precision Technology
 - 2.15 Samsung Electro-Mechanics
 - 2.16 Shinko Electric Industries Co., Ltd.
 - 2.17 3M Company
 - 2.18 UniMicron Technology Corporation
- 3 Flip Chip Substrate Users**
 - Altera, LSI Logic Corporation, Sun Microsystems, Xilinx
- Appendix: Substrate Suppliers**

List of Figures

- 1.1. Metal price trends.
- 2.1. ASE's RoHS compliance schedule.
- 2.2. Fujitsu's GigaModule-4 substrate.
- 2.3. 3M's substrate roadmap.
- 3.1. Weibull plot of solder joint failures.

List of Tables

- 1.1. QFP Assembly Prices
- 1.2. Wire Bond PBGA Assembly Prices
- 1.3. Flip Chip PBGA Assembly Prices
- 1.4. Laminate CSP Assembly Prices
- 1.5. Lead Frame CSP Assembly Prices
- 2.1. Japan's Solder Bump Trends
- 2.2. Japan's Environmental Trends
- 2.3. Flip Chip Substrate Finishes
- 2.4. Laminate Flip Chip Substrate Sources
- 2.5. ASE's Substrate Capacity Plan
- 2.6. Design Rules for ASE
- 2.7. Design Rules for Daisho Denshi
- 2.8. Design Rules for EI
- 2.9. Fujitsu Interconnect Technologies' Flip Chip Substrates
- 2.10. Design Rules for Fujitsu
- 2.11. Design Rules for Ibiden
- 2.12. Design Rules for JCI
- 2.13. Design Rules for Kinsus
- 2.14. Design Rules for Kyocera
- 2.15. Design Rules for Mitsui Chemicals
- 2.16. Design Rules for TNCSi
- 2.17. Design Rules for Nan Ya PCB
- 2.18. Design Rules for NTK
- 2.19. Design Rules for PPT
- 2.20. Design Rules for Shinko
- 2.21. Design Rules for 3M
- 2.22. Design Rules for UniMicron
- 3.1. Flip Chip Substrate Surface Finishes
- 3.2. LSI Logic's Evaluation of Underfills
- 3.3. LSI Logic's Flip Chip Package Features
- 3.4. Package Characteristics in Sun's Solder Joint Integrity Study


TechSearch
INTERNATIONAL

4801 Spicewood Springs Road • Suite 150
Austin, Texas 78759
Tel: 512-372-8887 • Fax: 512-372-8889
tsi@techsearchinc.com • www.techsearchinc.com