



BGA/CSP DEVELOPMENT UPDATE SERVICE

Third Quarter, 2002

The third quarterly BGA/CSP update for 2002 features special coverage of the drivers for electronics manufacturing growth in China. A section on new IC package substrate developments is provided, including coverage of Phoenix Precision Technology's new flip chip production line and STI's substrate production in China and its new flip chip package. An analysis of new developments in wafer level testing is provided. New package developments such as stacked packages, bumpless flip die packages for memory devices, and LSI's introduction of wire bonding on active surface area are detailed.

Table of Contents

- 1 Drivers for China's Growth
- 2 IC Package Substrate Developments
 - 2.1 Substrate Technology, Inc.
 - 2.1.1 Co-Development Work with Amkor
 - 2.1.2 STI's China Facility
 - 2.1.3 STI's Flip Chip Substrate
 - 2.2 Phoenix Precision Technology's New Flip Chip Substrate Line
- 3 Testing at the Wafer Level
 - 3.1 Wafer Level Burn-in Testing
 - 3.1.1 ChipMOS WLBT Service
 - 3.1.2 Aehr Test WLBT System
 - 3.1.3 FormFactor's WLBT Contactor
 - 3.1.4 SCS Hightech, Inc.
- 4 New Package Developments
 - 4.1 LSI Logic's Pad on I/O™
 - 4.2 Bridge Semiconductor's Low Cost Bumpless Flip Die Packages
 - 4.3 STMicroelectronics Introduces Thermally Enhanced BGA for HDDs
 - 4.4 New Stacked Packages
 - 3.5. Effect of burn-in time on burn-in cost for different approaches.
 - 3.6. Projected roadmap of cost of WLBT vs. package processing.
 - 3.7. Development roadmap for ChipMOS WLBT.
 - 3.8. FormFactor high temperature probing on solder bumps.
 - 3.9. SCS Hightech's Vertical Probe Card.
 - 3.10. SCS Hightech's probe tip.
 - 3.11. Bumps after probing.
 - 3.12. SCS Hightech's carrier for burn-in test.
 - 4.1. Three-row wire bonding of 3-deep on-chip pad bonded.
 - 4.2. Pad on I/O™ technology.
 - 4.3. Bumpless flip die package versus standard packages.
 - 4.4. Bridge Semiconductor's package.
 - 4.5. Fine line Ni/Cu/Ni traces plated on a copper carrier with 50µm line and spaces.
 - 4.6. Fine-line Ni/Cu traces on copper carrier.
 - 4.7. Vias formed to expose the die pads.
 - 4.8. A completed trace-to-pad interconnect by electroplating process.
 - 4.9. A resin-filled copper bump.
 - 4.10. Bridge Semiconductor's process flow.
 - 4.11. C2BGA cross section.
 - 4.12. Mitsubishi Electric's stacked CSP process.

List of Figures

- 2.1. Cross section view of STI's substrate with two-circuit layers.
- 2.2. Insertion loss and return loss.
- 2.3. STI's China facility.
- 2.4. STI's Electra FCBGA substrate cross section (2+2 layer pair).
- 2.5. STI's Ultra-BGA™ substrate.
 - 3.1. Cost of WLBI vs. package BI.
 - 3.2. Cost of WLT vs. package test.
 - 3.3. Effect of volume on burn-in cost for different approaches.
 - 3.4. Effect of product life on burn-in cost for different approaches.

List of Tables

- 2.1 Design Features for STI Substrates
- 2.2 STI Substrate PID Electrical Characteristics
- 2.3 Attributes of the OC-48 and OC-192 Performance Envelope
- 2.4 Manufacturing Tolerances Affecting the Electrical Design
- 2.5 PPT's Build-up Substrate Design Rule Development Roadmap
 - 3.1 Back-end Flow Comparison of WLBT and Package Burn-in and Test