





TechSearch International, Inc.

Corporate Overview

E. Jan Vardaman, President

-  TRACK INNOVATION
-  IDENTIFY TRENDS
-  ANALYZE GROWTH
-  INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY

Corporate Background

- **Founded in 1987 and headquartered in Austin, Texas**
- **Recognized around the world as a leading consulting company in the field of advanced packaging technology**
- **Specialists in advanced semiconductor packaging and assembly, electronics manufacturing, and materials**
- **What sets TechSearch International apart from others?**
 - ✓ We have close relationships with companies and industry leaders built on trust and mutual respect
 - ✓ We ask customers what they want—report content is constantly tailored to meet those needs
 - ✓ We provide complete, concise, accurate data, and unbiased opinions
 - ✓ We participate in many industry conferences to share our findings and stay up-to-date on the latest innovations
 - ✓ We frequently tour PCB, EMS, and OSAT manufacturing facilities

1987 ————— YEARS OF TECHSEARCH INFLUENCE ————— Now

How can we help you?...Our Mission

- **Enable clients to capitalize on opportunities for profitable growth with our**
Accurate → Relevant → Timely → Market and technology analysis
- **Provide tools that enable success:**
 - ✓ Authentic technical and economic analysis of market and technology trends in semiconductor packaging, assembly, and materials
 - ✓ Frequent updates on the latest technology developments
 - ✓ Strategic planning and execution assistance
 - ✓ Technology licensing and connecting partners for joint development
 - ✓ Cost analysis with software models
- **Participate directly with client teams in providing an understanding of changes and drivers in the marketplace**
- **Provide competitive analysis of semiconductor packages, materials, and assembly equipment marketplaces to aid new product introductions**



Market analysis you can trust!...Multi-client reports



- **Flip Chip and WLP Market and Technology Analysis**
- **New Packages and Materials for Power Devices**
- **New Frontiers in Automotive Electronic Packaging**
- **SiP for Mobile and Wearable Applications**
- **Global Semiconductor Packaging Materials Outlook**
PARTNERSHIP WITH SEMI
- **Worldwide OSAT Manufacturing Sites Database**
PARTNERSHIP WITH SEMI
- **3D IC Gap Analysis: Remaining Issues, Solutions, Market Status**
- **Advanced Packaging Cost Models and Analysis**
PARTNERSHIP WITH SAVANSYS
- **Advanced Packaging Update (4 issues each year)**
 - Economic and business developments in the semiconductor packaging and assembly industry including market forecast by package type (FBGA, FLGA, QFN, stacked die CSP, PoP, etc.)
 - New packages and materials including trends and drivers
 - Various market and technology analysis

Market analysis you can trust!...Single-client reports



- Silicon and glass interposers
- Materials for 3D TSV bond/debond
- Flex circuit for medical electronics
- Power device makers
- 3D integration technologies
- Thin wafer dicing market/laser dicing
- IC package and bump inspection
- Trends in mobile phone packaging
- Test sockets
- Probe cards
- Dielectric materials for IC packaging, including bumping and wafer level packaging
- Underfill materials for flip chip and WLP
- Memory packaging trends
- Thermal interface materials
- Flip chip and wire bonding equipment
- Pb-free solder material
- and more!

At the forefront...Recognizing emerging trends

- **Automotive Electronics**

First industry analysis of packages for automotive electronics with a focus on ADAS

- **Flip Chip Trends**

Publishing reports on flip chip markets and technology trends since 1994 — We've done cutting edge analysis in recognition of the shift to Cu pillar

- **WLP Demand and Capacity**

Tracking wafer bump and WLP capacity and demand trends since 2003 — We've been at the front in recognizing the shift to fan-out WLP (FO-WLP)

- **Ball Grid Arrays and Chip Size Packages**

First industry analysis of the ball grid array market in 1994 — We've published annual forecasts of BGA and CSP demand ever since

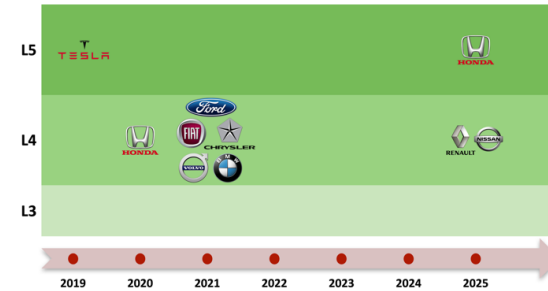
- **3D IC with TSVs and Si Interposers**

We are recognized as the provider of realistic market forecasts — We are unique in offering gap analysis, with indications of key areas requiring additional work

- **System-in-Package and Multichip Modules**

Tracking markets and trends since 1990

Timeline for Roll Out of Autonomous Vehicles



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Growing Number of FO-WLP Applications
(Red is Panel Potential)

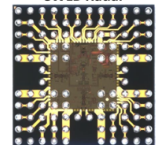
- Baseband/Application processors
- RF transceivers and modules, switches
- Power management integrated circuits (PMIC)
- Connectivity modules (IoT)
- Radar modules (77GHz) for automotive
- Audio CODECs
- Microcontrollers
- Logic + memory
 - Data center servers, networking, AI etc. (Fan-out on substrate)
 - Future AP + DRAM for mobile
- Sensors (fingerprint, image, etc.)
- LED
- Controller for flash memory stack/SSD
- Many multi-die configurations

Qualcomm Audio CODEC



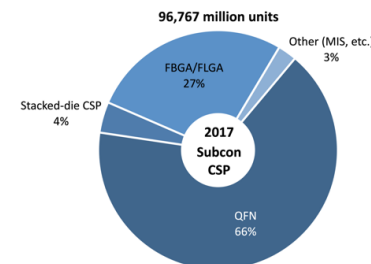
Source: TechInsights

eWLB Radar



Source: Infineon.

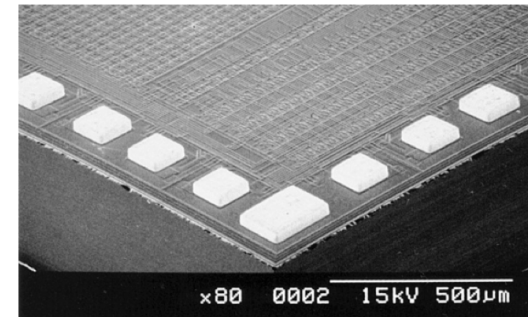
Subcontractor CSP Units by Package Type



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Technology Licensing Examples

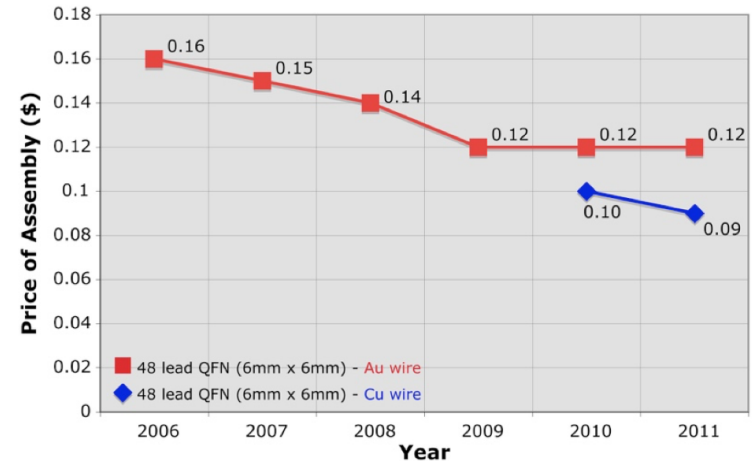
- **NTT's copper polyimide thin film technology from Japan to the United States**
- **Matsushita's TBTAB technology**
- **Aptos gold bump technology from the United States to Taiwan**
- **Tessera's μ BGA technology from the United States to Korea**
- **Flip chip assembly and solder bumping technology**
- **3D Plus stacking technology**
- **Beltronics inspection technology from the United States to Japan**



Cost Analysis Software Models

Wire Bond, Flip Chip, and Wafer Level Package Models

- Wire bond cost analysis
 - Copper versus gold wire trade-offs
- Flip chip cost analysis
- WLP and FO-WLP cost analysis
- Collaboration with SavanSys Solutions
 - SavanSys develops model software
 - TechSearch helps with model calibration

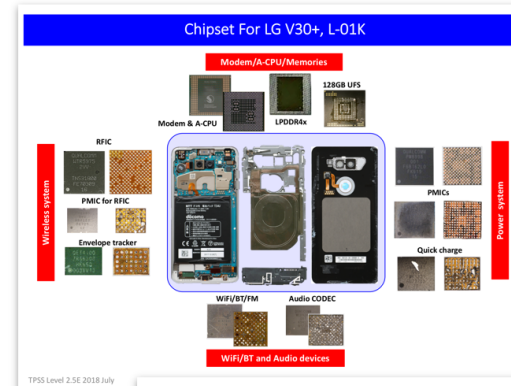


2.5D and 3D Packaging Cost Model

- After successful collaboration on cost models for other packaging technologies, SavanSys and TechSearch introduced a cost model for 2.5D and 3D packaging
- The first cost model to cover the total cost and yield from fabrication of the wafer to complete assembly, for both 2.5D and 3D
- Detailed manipulation of the process flow to meet user requirements is possible

System Teardown Reports

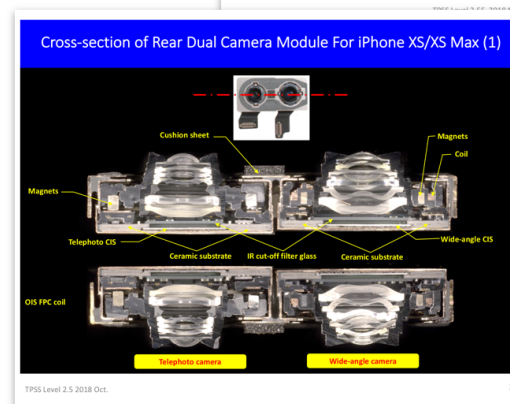
- TechSearch markets system teardown reports from Total Process Solution Study Group (TPSS). TPSS was started in mid-2003 by engineers in Japan involved in the assembly and Jisso technology for advanced portable equipment such as cellular phones and digital still cameras. Today, TPSS provides technology and detailed teardowns of smartphones, tablets, wearables, game consoles, drones, and more.
- The reports typically contain details such as:
 - Photographs of circuit boards and components
 - Component information such as vendor, type of package, size, lead count, pitch
 - X-ray images of packages
 - Detailed analysis of displays and camera modules
 - Printed circuit board (PCB) construction information



Details of Key Semiconductor/Electronic Devices (12)

No.	01	02	03
Manufacturer	ST Microelectronics	AKM	Murata
Part number	SF 748	7A16 ACC	10W KM819051 A18 DMAJ24
Function	Accelerometer + gyroscope	Electronic compass	WiFi/BT/M module
Package type	FLGA14 in 0.50mmP	WLP5 in 0.40mmP	FLGA124 in 0.43mmP
Package size	3.03x2.51x0.86mm	0.80x1.21x0.35mm	8.80x7.64x1.11mm
Package pictures			
X-ray pictures			

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Workshops, Conference Presentations, and Exhibitions

- **Workshops on relevant topics such as wearables, medical electronics, flip chip, 3D TSV, embedded components, optoelectronics, automotive electronics, and substrates**
 - Periodic topical workshops in Austin, Texas
 - Together with the Fraunhofer Institute, we host a workshop in Munich, Germany, the day before Productronica
- **Recent Conference Presentations and Exhibitions**
 - *IMAPS International Conference on Device Packaging* – Fountain Hills, Arizona
 - *NEPCON Japan, IC & Sensor Packaging Technology Expo* – Tokyo, Japan
 - *Heterogeneous Integration: The Path Forward* – Milpitas, California
 - *International Wafer Level Packaging (IWLPC)* – San Jose, California
 - *IMAPS International Symposium on Microelectronics* – Pasadena, California
 - *Strategic Materials Conference (SMC)* – San Jose, California
 - *Electronics System-Integration Technology Conference (ESTC)* – Dresden, Germany
 - *IEEE Electronics Components and Technology (ECTC)* – San Diego, California
 - *International Conference on Electronic Packaging (ICEP)* – Kuwana, Japan
 - *ADAS Sensors Conference and Exhibition* – Detroit, Michigan
 - *SEMICON China, SEMICON Europa, SEMICON Taiwan, SEMICON West*

Thank you!

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